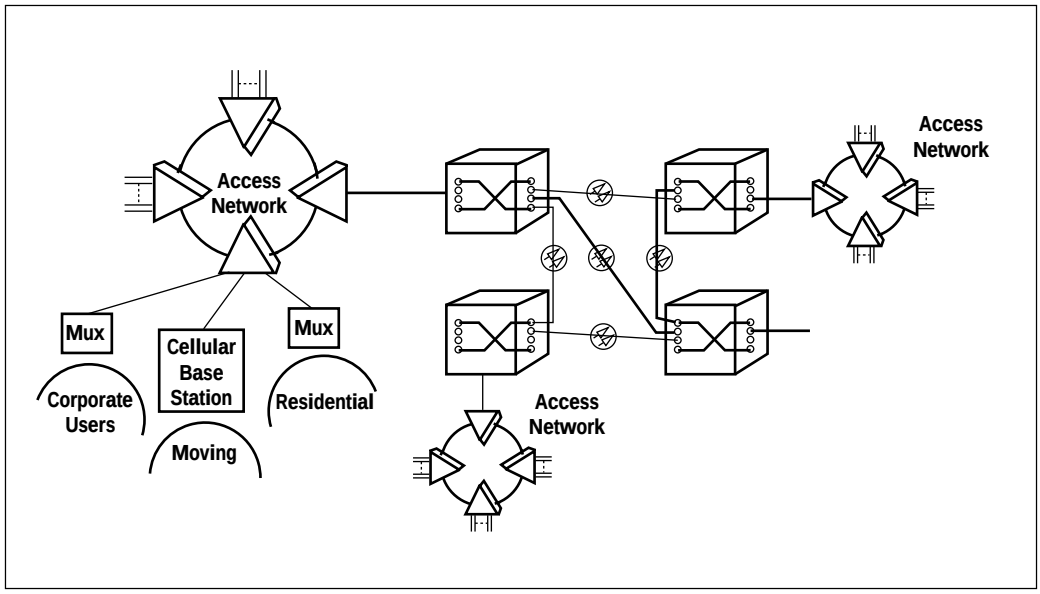
HEWLETT® PACKARD

Synchronizing Telecommunications Networks:

Synchronizing SDH/SONET

Application Note 1264-2



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I. Introduction

Synchronous Digital Hierarchy (SDH) and Synchronous Digital Network (SONET) are new transmission systems that provide for standardized high-speed optical transport. The goal of SDH and SONET is to provide ease of networking, intervendor compatibility, standardized interfaces, and standardized overhead for operations, administration, maintenance, and provisioning.

With the introduction of SDH and SONET, new demands are placed on network synchronization. The synchronization performance of most telecommunications networks require improvement to support SDH and SONET. For the first time, short-term performance (timing stability for durations up to 1,000 seconds) becomes important. This necessitates the use of excellent clocks. Long-term performance also requires scrutiny, as many administrations begin to utilize multiple Primary Reference Source (PRS) clocks and shorten synchronization chains to keep wander to a minimum. All these actions are necessary to maintain error-free transmission of DS1, E1, and DS3 signals that pass through SDH and SONET.

Section II of this application note provides the basic background on SDH and SONET necessary to understand the synchronization issues presented by each system. Section III covers network synchronization performance and its impact on SDH and SONET. The impact that SDH and SONET have on current Plesiochronous Digital Hierarchy (PDH) transport is presented in Sections IV and V. Section IV focuses on the issues of DS3 transport through SDH and SONET systems and Section V describes the impact on DS1 and E1 transport. The network synchronization requirements to support an SDH network are considered in Section VI, while the needs for SONET are given in Section VII.

The basic synchronization principles of SDH and SONET are identical. Therefore, when describing common attributes, this application note will refer to both systems as SDH/SONET. There are, however, differences in the architecture and implementation of networks using each system. When only one system is being referred to, it will be given explicitly by name.

Two additional Hewlett-Packard application notes provide background information on network synchronization. See reference items [1] and [2] on page 24.

II. SDH and SONET Transmission Basics

This section presents the basic transmission concepts of SDH and SONET which are necessary to understand their synchronization. Both SDH and SONET synchronously multiplex their signals. This allows two major advantages over current asynchronous systems: single-step multiplexing and cross-connect and add-drop functionality.

In current asynchronous systems, to obtain higher rate signals, the system must multiplex the signal at each level of the transmission hierarchy. For example, DS1 signals are multiplexed into DS2, then DS2 to DS3, then DS3 to proprietary optical rates. In SDH/SONET, multiplexing is done in one step, since the signal is synchronous.

The second major advantage is cross-connect and add-drop capability. In order to obtain a DS1 or E1 in current asynchronous systems, the entire signal must be de-multiplexed. The optical rate must be de-multiplexed to a DS3, the DS3 to a DS2, the DS2 to a DS1 or E1. You must obtain all DS1s or E1s in order to obtain a single one. In SDH/SONET the DS1 or E1 can be obtained directly without de-multiplexing the entire signal.

SDH Multiplexing

The 155.520 Mbps Synchronous Transport Module - Level 1 (STM-1) is the basic rate for SDH [3]. All lower rate payloads, such as DS1, E1, and DS3, are mapped into an STM-1 [4]. Higher rate signals are obtained by multiplexing N STM-1s into an STM-N. No additional overhead or processing is used to create an STM-N from STM-1 signals. The STM-1 signal is composed of either three Administrative Unit Level 3 (AU-3) signals or one AU-4 signal.

Payloads may be mapped into SDH in several ways. See Figure 1 on page 6. A DS1 or E1 signal is first mapped into a Virtual Container (VC-11, VC-12, respectively). This VC contains the payload plus overhead information. The VC-11 or VC-12 is then mapped into a higher rate VC, such as VC-3, which can also be used to carry DS3 signals. The VC-3 signal has additional overhead information. The higher rate VC is then mapped into the AU-3 or AU-4 signal of which the STM-1 is comprised.

SONET Multiplexing

SONET is similar to SDH, but it uses different building blocks for its transport [5]. The 51.84 Mbps Synchronous Transport Signal - Level 1 is the basic building block of SONET. Lower rate payloads are mapped into STS-1. Multiple STS blocks are multiplexed to form an STS-N.

In SONET, DS1 payloads are first mapped into Virtual Tributaries, called VT1.5 (Figure 2). The VTs are similar to the SDH VC in that they contain the payload plus overhead information. The VT1.5s are then mapped into the STS-1 SPE. DS3 payloads are mapped directly into an STS-1 SPE.

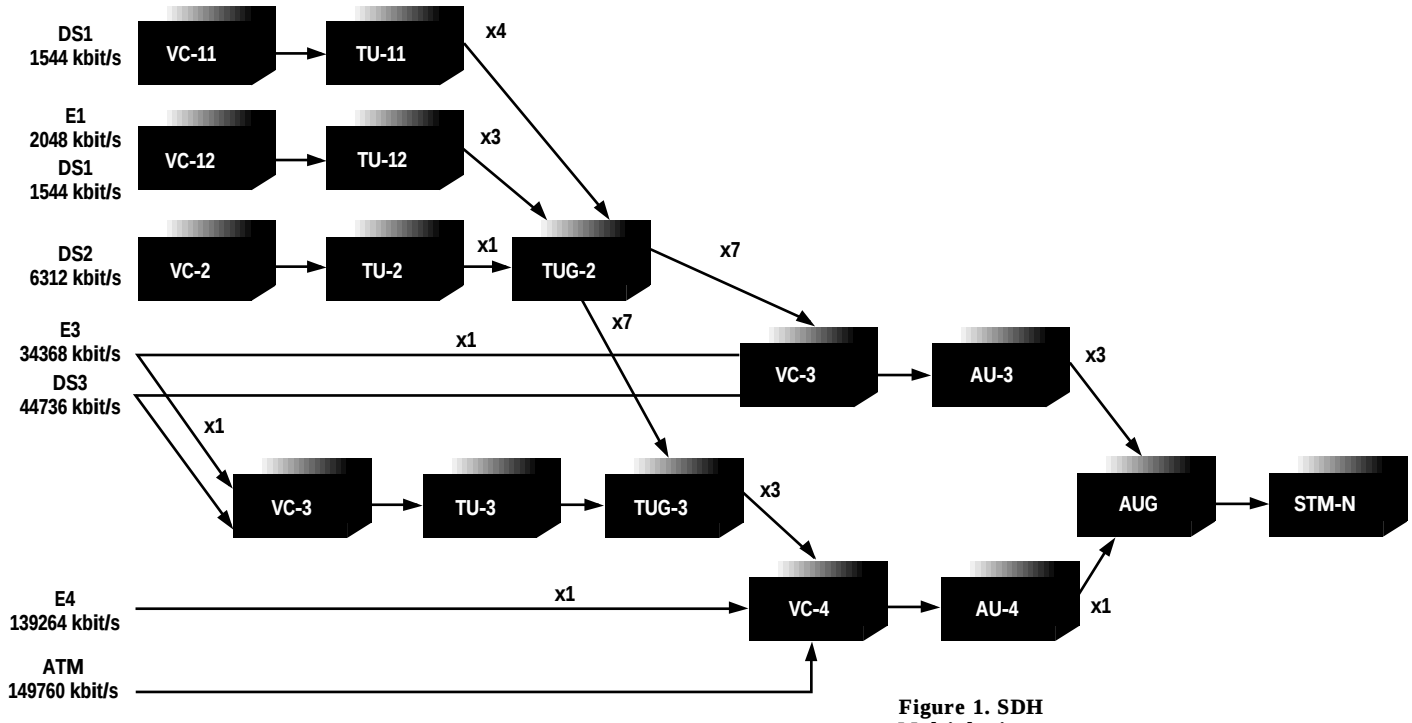


Figure 1. SDH Multiplexing.

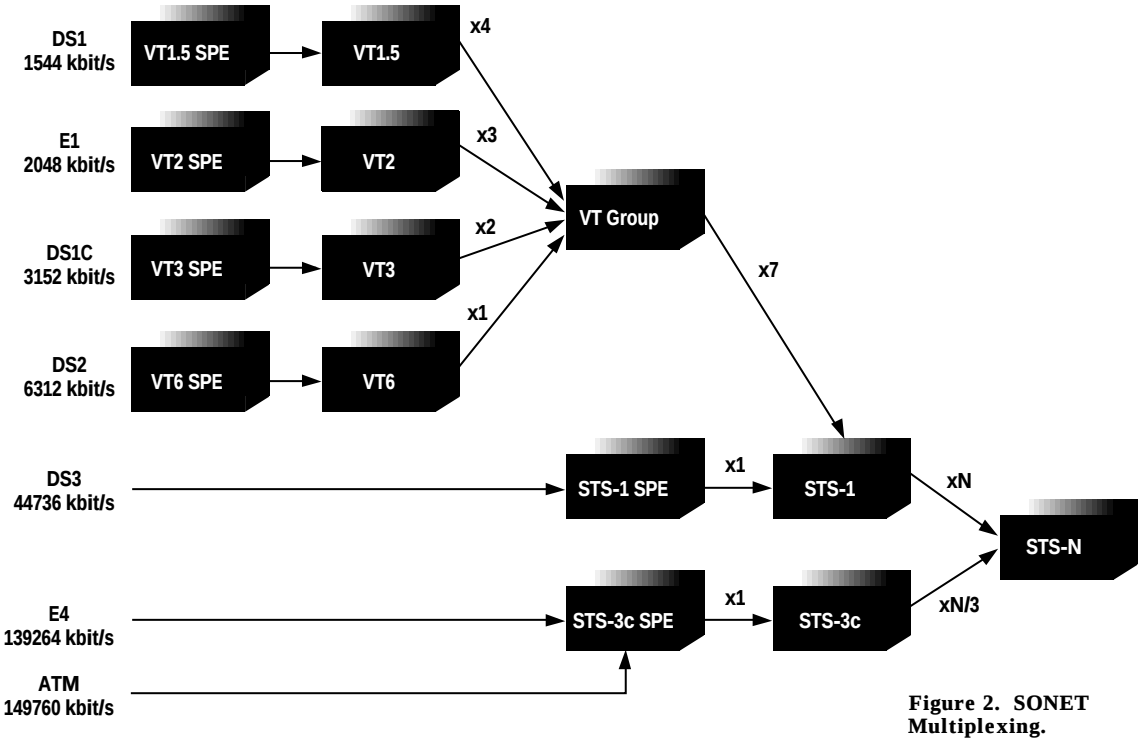


Figure 2. SONET Multiplexing.

Pointers and Pointer Adjustments

Both SDH and SONET utilize payload pointers to carry the signal. The payload pointer gives the location of the beginning of the payload within the SDH/SONET structure.

Differences in phase and frequency between two SDH/SONET NEs (Network Elements) can be handled by the use of payload pointers. If the sending SDH/SONET NE is faster than the receiving NE, the receiving NE will introduce a negative pointer adjustment and shift the payload ahead by one byte or 8 bits. See Figure 3 on page 8. In this manner, the receiving NE can keep up with the sending NE without loss of information. Similarly, if the sending NE is slower than the receiving NE a positive pointer adjustment of one byte is introduced. See Figure 4 on page 9.

Payload Mapping

DS3 signals are mapped into SDH/SONET by using stuffing bits to account for the variations in timing between the DS3 and the SDH/SONET system.

DS1 and E1 signals can be mapped using one of four methods [4, 5, 6]: Asynchronous mapping, Floating Byte Synchronous mapping, Locked Byte Synchronous mapping, and Bit Synchronous mapping.

In asynchronous mapping, the DS1 or E1 signal is mapped into the VT1.5 or VC-12/13 asynchronously using stuff bits to accommodate timing differences. Pointers are used to indicate the beginning of the VT/VC frame. With asynchronous mapping, the DS1 or E1 signal is transported without slips and without retiming of the signal. It will, however, be subject to pointer adjustments which occur due to any frequency differences between SDH/SONET NE in the transmission path.

Floating byte synchronous mapping differs from asynchronous mapping in that it does not include stuff bits to accommodate timing differences between the payload and the NE. This mapping allows direct access to DS0 signals. However, it requires that the DS1 or E1 be locked to the SDH/SONET NE. Any frequency difference between the incoming payload and the first SDH/SONET NE in the transport will cause slips.

Locked byte synchronous mapping does not allow for any stuff bits or pointers in the mapping process. Therefore, the DS1 or E1 must be locked to the SDH/SONET NE. A slip buffer must be provided to accommodate timing differences throughout the transport.

Bit synchronous mapping is the same as locked byte synchronous mapping except that it does not assume that the DS1 or E1 structure is organized into DS0s. The DS1 or E1 is passed as a single bit stream with or without DS0 or DS1/E1 frames.

It is expected that the majority of networks will use asynchronous mapping to transport DS1 and E1 signals.

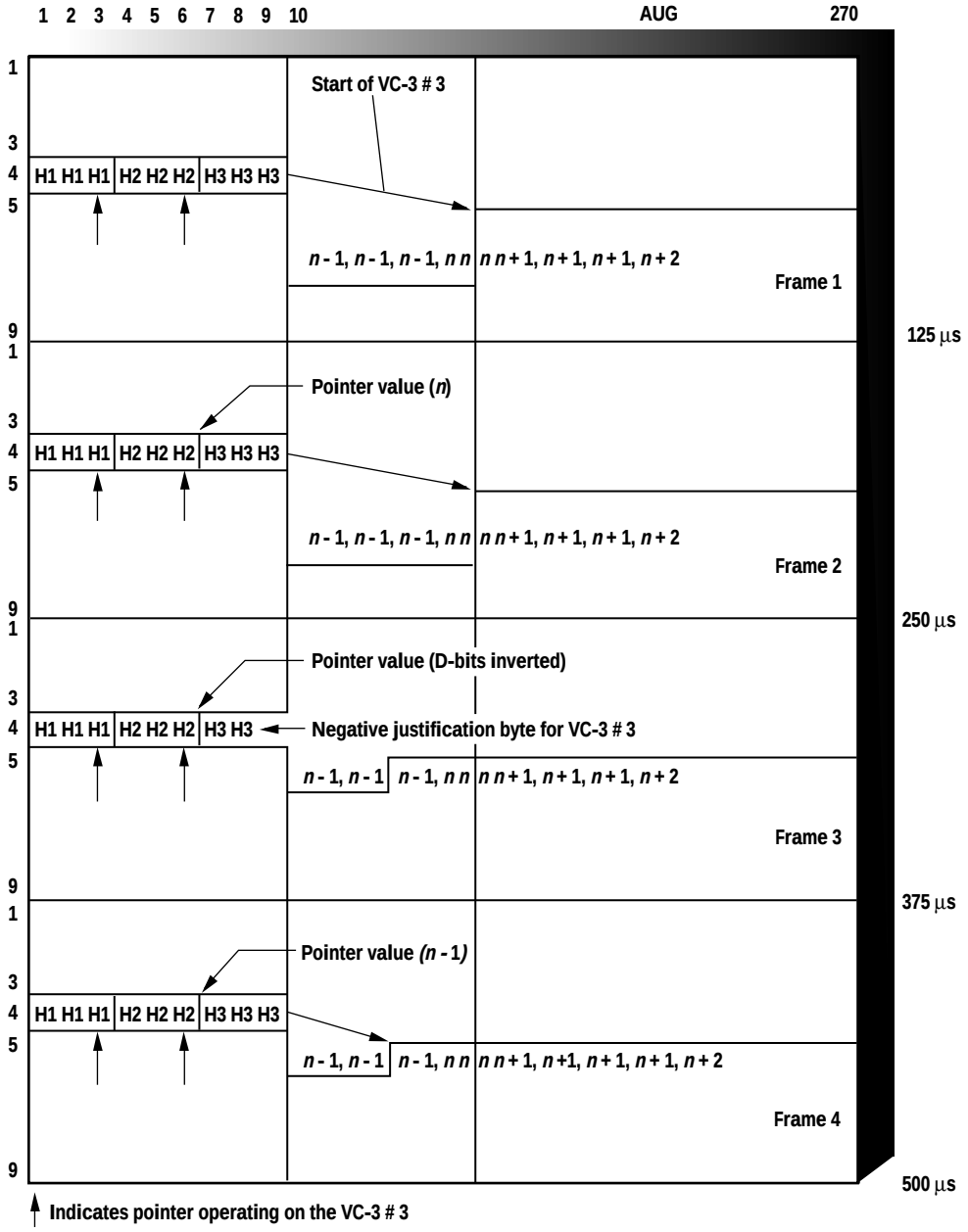


Figure 3. AU-3 pointer adjustment operation — negative justification.

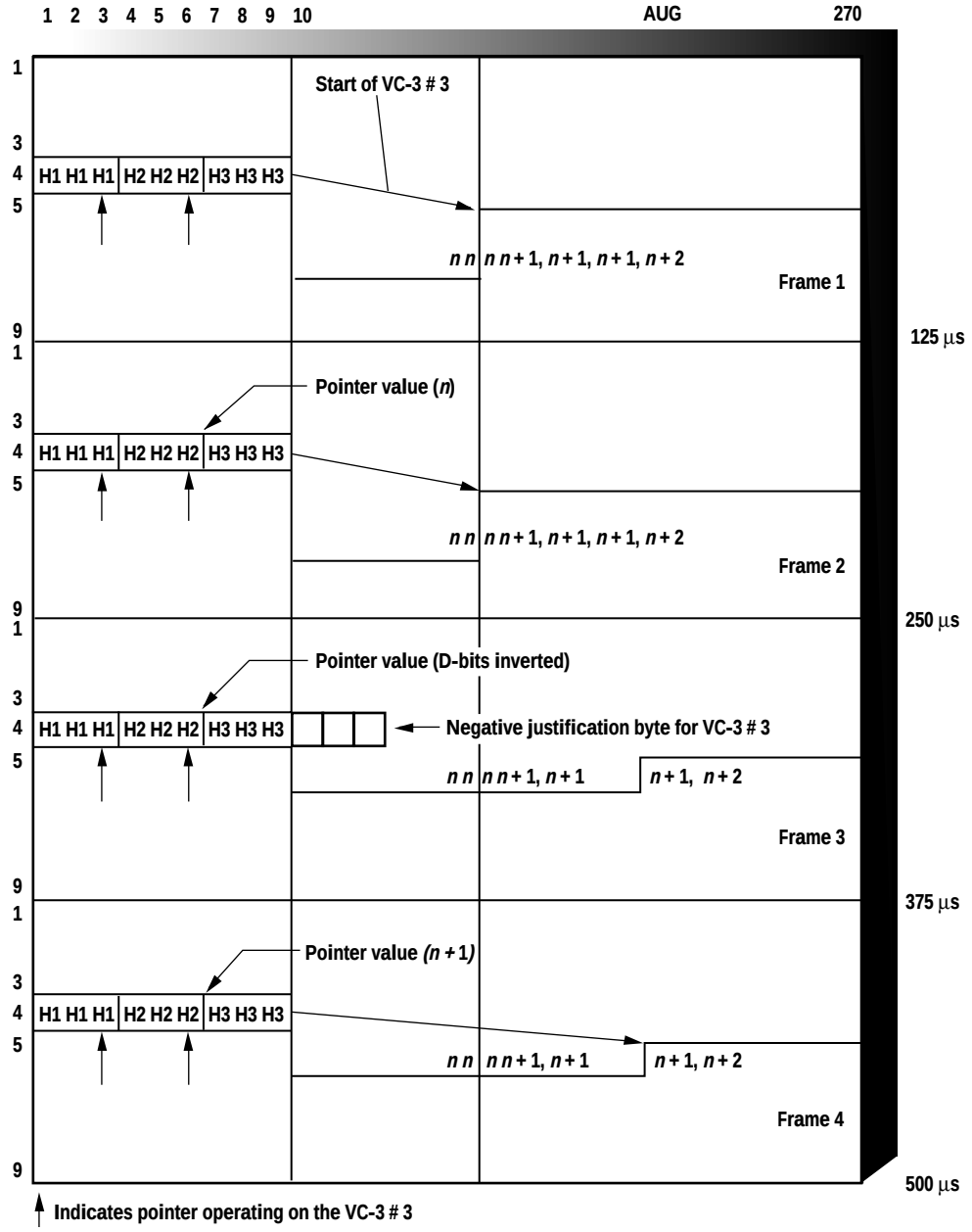


Figure 4. AU-3 pointer adjustment operation — positive justification.

III. Synchronization Performance and Sources of Pointer Adjustments

Pointer adjustments occur when the sending SDH/SONET Network Element's (NE's) timing is different than the receiving SDH/SONET NE's timing. The synchronization performance at any one element in a network is typically characterized by three components: the accuracy of the master clock, the performance of the facilities distributing the reference, and the performance of the receiver clocks obtaining a reference over the facilities [1]. The synchronization inaccuracy of the master clock usually contributes a small portion of the timing inaccuracies in a synchronization network [1]. Synchronization performance is dominated by a combination of the facility and receiver clock performance.

The receiver clock performance can be characterized by its operation in three scenarios [7]:

– Ideal Operation
– Stressed Operation
– Holdover Operation

Ideal operation describes the short-term behavior of the clock and is important to control pointer adjustments in SDH and SONET networks. Stressed operation is the typical mode of operation of a receiver clock, where a receiver clock is expected to receive timing from a source clock over a facility that has short-term impairments. Finally, holdover operation characterizes the clock's performance in the rare case when all timing references to the clock are lost.

The major sources of pointer adjustments correlate with these modes of clock operation. Under ideal operation, the clock produces random phase movements which greatly contributes to DS3 pointer adjustments. Stress operation of network clocks causes an accumulation of phase errors in a network which can be a major cause of DS1 and E1 pointer adjustments. Lastly, holdover operation will cause a steady stream of DS3, E1, and DS1 periodic pointers.

Ideal Operation and Random Phase Movements

In ideal operation, the receiver clock experiences no interruptions of the input timing reference. Even though this is not typical of real network operation, understanding a clock's performance under ideal operation gives bounds for the clock's performance. It also indicates the short-term noise of a clock, which will impact the occurrence of DS3 pointer adjustments in SDH/SONET networks and the resulting SDH/SONET DS3 payload jitter.

Stressed Operation

This category of operation reflects the performance of a receiver clock under actual network conditions where short interruptions of the timing reference can be expected. The number of interruptions can range from 1 to 100 per day.

All interruptions will affect the receiver clock. During the interruption, the timing reference cannot be used. When reference is restored or if the interruption persists and the clock switches references, there is some error regarding the actual time difference between the local receiver clock and the newly restored reference. The timing error that occurs due to each interruption depends on the clock design, but it should be less than 1 microsecond [8, 9].

A timing error of 1 microsecond can cause up to seven DS3 pointer adjustments. These seven pointer adjustments can occur in a very short period of time. The SDH/SONET NE is designed to handle this without introducing errors on the payload DS3.

A single stress event will not affect DS1 or E1 transport through SDH/SONET, since 4.6 and 3.5 microseconds of timing error are required to cause DS1 or E1 pointer adjustments, respectively. Unfortunately, the timing errors due to stress will accumulate [1]. This accumulation of timing errors is a major cause of DS1 or E1 pointers.

Holdover Operation

A receiver clock will operate in holdover in the rare case that it loses all its timing references for a significant period of time. There are two main contributors to holdover performance: initial frequency offset and frequency drift. Initial frequency offset is caused by the settability of the local oscillator frequency and the noise on the timing reference when the clock first enters holdover. Frequency drift occurs due to aging of the quartz oscillators.

If the SDH/SONET NE is in holdover or locked to another clock that is in holdover, there will be a steady accumulation of phase errors. In this case, a steady stream of pointer adjustments will occur. The rate at which these pointer adjustments occur will increase as the frequency of the holdover clock drifts.

IV. Synchronization Effect of SDH/SONET on Payload DS3s

SDH/SONET can affect DS3 transport, even though it is asynchronous [1]. This is due to the payload pointer adjustments. A change in payload pointer reflects a change in the position of the payload by one byte or 8 UI. (A UI, or unit interval, is the duration of time needed to send a single bit.) This is incompatible with current DS3 systems since they are designed to accept only 5 UI of jitter. Only 5 UI of sudden phase movement are allowed on the input to DS3 equipment. If this 5-UI specification is exceeded, the DS3 equipment may not be able to read the data input and will cause an error in transmission.

It is necessary for the SDH and SONET equipment to slow down (filter) the phase movement caused by a pointer adjustment so that the receiving DS3 equipment can accept the signal without error. However, if the SDH/SONET equipment slows down the phase movement too much, it may begin to overlap with the phase movement caused by the next pointer adjustment. Engineering an SDH/SONET network requires that limiting the occurrence of pointer adjustments be balanced against restricting the SDH/SONET filtering requirements. The former places demands and expense on the network synchronization performance; the latter puts the demands and expense on the SDH/SONET equipment.

As a general trend, ANSI has been specifying SONET insofar as it will work in current networks with minimal changes. Therefore, it has been placing more demands on the SONET equipment. ETSI and ITU, in general, have taken a slightly different approach and placed fewer synchronization demands on the SDH equipment and more on the network.

Amount of Pointer Adjustments in a Network

The number of pointer adjustments in the network can be understood by considering operation in the three scenarios given in Section III: ideal, stress, and holdover operations.

Under ideal operation, all clocks in the synchronization network exhibit some random phase movement. Simulations have been done based on typical random phase movement measured in telecommunication networks. They have shown that pointer adjustments on DS3 payloads can occur every 20 to 100 seconds. The number of DS3 pointer adjustments is highly dependent on the short-term (less than 1,000-second) timing stability in the network. In addition, it was found that there could be up to three pointer adjustments occurring simultaneously.

A second major cause of timing inaccuracy is stressed operation on network clocks and the resulting clock rearrangements. The timing error caused by a clock rearrangement is limited to 1 microsecond [8, 9]. However, such a phase movement can cause up to seven DS3 pointer adjustments. These seven pointer adjustments can occur in a very short period of time. The SDH/SONET NE must be able to spread these adjustments out so that the DS3 payload leaving the NE does not experience more than 5 UI of jitter. The number of such events can range from 1 to 100 per day, depending on the network architecture and facility performance.

Clock holdover is a third cause of timing inaccuracies between clocks. With a clock in holdover, the clock's timing will drift from the timing of the network. This will cause a steady stream of pointer adjustments to occur on the payload. For SONET NEs, pointer adjustments may occur every 34 milliseconds when the NE is in holdover. For SDH NE, they occur every 320 milliseconds.

Jitter Introduced by SDH/SONET on Payload DS3s

In order to maintain the 5-UI jitter requirement on DS3 payloads, ANSI has specified the amount of jitter that SONET introduces on the payload [10]. Table 1 gives the DS3 jitter requirements of ANSI. It should be noted that all entries in the table include jitter caused by DS3 mapping.

Table 1. ANSI DS3 Jitter Requirements for SONET Interfaces

Mapping	0.4 UI
Single Pointer	0.7 UI
Triple Pointer Bursts	1.3 UI
Phase Transient	1.2 UI
Periodics	1.0 UI
Periodics + Single Pointer	1.3 UI

The jitter levels are given for each situation described in the previous sections. Mapping jitter, single pointer jitter, and triple pointer bursts cover the ideal operation situation. The phase transient requirement covers clock rearrangements. Finally, jitter during clock holdover operation is given by the periodics listing.

Network Requirements to Support SDH/SONET with DS3 Traffic

The network requirements to support DS2 traffic through SDH/SONET are geared towards reducing the number of DS3 pointer adjustments. The three major sources of pointer adjustments are again considered.

To limit random phase movements and the resulting pointer adjustments, the short-term noise of the network synchronization clocks must be limited.

ANSI requires that the band-limited short-term noise at the output of any clock not exceed 100 nanoseconds [8]. In addition, the band-limited short-term noise from a BITS clock should not exceed 17 nanoseconds. This implies that the network operates at the Bellcore stratum 3E [11] or ITU local clock performance levels and that synchronization chains in the network are limited.

Some administrations have actively pursued reducing the number of clock rearrangements and their impact on SDH/SONET, although these are not absolutely necessary for DS3 transport. To reduce their numbers, synchronization chains are shortened, more primary reference clocks are used in the network, and/or selected high-performance, low-error facilities are used in the synchronization network. To reduce the impact of rearrangements, some administrations are requiring clocks with better than 1 microsecond rearrangement [11], while ETSI and ITU are proposing that network clocks have slower responding rearrangements, spreading out the seven pointers that may occur.

The impact of clock holdover is not an issue. Clocks rarely enter into holdover for periods of more than a few minutes, as long as diverse references are supplied [1]. The network only requires that stratum 3 holdover (for SONET networks) and local clocks (for SDH networks) be used.

V. Synchronization Effect of SDH/SONET on Payload DS1s and E1s

The effect of SDH/SONET on payload DS1s and E1s is different than its impact on DS3 signals. A pointer adjustment on a DS1 or E1 causes an 8 UI change of phase. This, like the DS3 case, is inconsistent with the requirement that DS1 and E1 equipment are designed to accept 5 UI of jitter. Therefore, the SDH/SONET equipment must slow down (filter) the pointer adjustment. The difference in the DS1 and E1 case is that DS1/E1 pointer adjustments do not occur often. Therefore, it is relatively easy to slow down one pointer adjustment without having it overlap with the occurrence of the next pointer adjustment.

An additional concern with DS1 and E1 payload through SDH/SONET is the wander that can occur. The accumulation of pointer adjustment events over time will cause wander on the payload DS1/E1. This is not a concern in the DS3 case, since DS3s are transmitted asynchronously.

Amount of DS1/E1 Pointer Adjustments in the Network

As with the DS3 pointer adjustment case, the number of DS1/E1 pointer adjustments is given by the three scenarios of Section III: ideal, stress, and holdover operations.

Simulations, based on random clock phase movement of clocks in ideal operation, has shown that DS1 pointer adjustments are expected to occur every 1,200 to 8,000 seconds on the DS1 payload. This is so seldom that it is unlikely for two pointer adjustments to occur at the same time.

Since clock rearrangements cause 1 microsecond of phase error or less, it takes several such events to accumulate enough phase error for a DS1 or E1 pointer adjustment. A DS1 pointer adjustment reflects 4.6 microseconds of timing difference, whereas E1 pointer adjustments are 3.5 microseconds. The number of DS1/E1 pointer adjustments caused by stress conditions is dependent on the number of clock rearrangements in the network. This, in turn, is highly dependent on network architecture, clock performance, and facility performance. The number of clock rearrangements can range from less than one per day to hundreds per day. Even in situations where the number of rearrangements is large, DS1/E1 pointer adjustments will occur as discrete individual events.

In clock holdover, even the worst network clock (stratum 3) will cause only one pointer adjustment every 12 seconds for a DS1 payload and every nine seconds for E1s. An SDH or SONET network element in holdover will cause a DS1 (E1) pointer adjustment every nine (seven) seconds. These are seldom enough that the adjustments will again appear as discrete individual events.

It is important to note that there are no mechanisms in the network that will cause phase movements large enough to require two simultaneous DS1/E1 pointer adjustments. Under all network operation conditions (ideal, stress, and holdover), only single discrete DS1/E1 pointer adjustment occurs.

Jitter Introduced by SDH/SONET on Payload DS1s and E1s

In order to maintain the 5-UI jitter requirement on DS3 payloads, ANSI has specified the amount of jitter that SONET introduces on the payload [12]. (See Table 2.) A portion of the 5 UI jitter into DS1 and E1 equipment will be caused by asynchronous DS3 transport in the network. ANSI allows 2.5 UI of jitter for the asynchronous portion of the transport. The remaining 2.5 UI is allocated for SONET transport. In Table 2, both ideal and stress operations are covered by the single pointer adjustment specification.

Table 2. ANSI DS1 Jitter Requirements for SONET Interfaces

Mapping	0.7 UI
Single positive pointer	0.6 UI
Single negative pointer	0.6 UI
Holdover positive pointers	0.6 UI
Holdover negative pointers	0.6 UI

Wander Introduced by SDH/SONET on Payload DS1s and E1s

The major impact of SDH/SONET on DS1 and E1 is wander. G. Garner [13] has shown that in typical transport networks, SDH/SONET can add 90 microseconds of wander per day onto the DS1/E1 signal. Wander of more than 18 microseconds can cause slips [1], although much DS1 and E1 equipment is designed to handle up to 90 microseconds of wander before incurring a slip. As a result, ITU [9] and EIA/TIA [14] require that wander on DS1 and E1 transport be limited to 18 microseconds.

To keep within this limit, ANSI has worked on a wander budget for a single DS1 line. This is given in Table 3. These wander figures are for DS1s intended for transport only. They are not intended to be applied to DS1 lines used for timing transfer.

Table 3. ANSI Daily DS1 Transport Wander Budget

Network switches	3.7 Microseconds
DS1 - DS3 mapping	0.3 Microseconds
DS1 - VT1.5 mapping	2.6 Microseconds
Fiber	1.3 Microseconds
SONET	10.1 Microseconds

Networks that just meet current ANSI [8] and ITU [9] synchronization performance requirements cannot achieve the 10.1-microsecond wander budget for DS1s transported by SONET. One method to meet the 10.1-microsecond budget is to improve network synchronization performance. Garner [13] found that the 10.1-microsecond budget can be met if the network is operated with performance that is between 10 and 100 times better than is currently specified by ANSI and ITU. This would require two major changes to a network. First, there would need to be better clock performance under ideal operation, especially in the 100- to 10,000-second range. Second, much tighter bounds on stressed operation performance are required.

Suitability for Timing Transfer

DS1 and E1 payloads that are transmitted by SDH/SONET are not suitable for passing timing from one location to another. There are several reasons for this. The first is because of the excessive wander that SDH/SONET introduces. Second, each pointer adjustment represents a sudden phase jump. For DS1 through SONET this phase jump is 4.6 microseconds. For E1 through SDH, it is 3.5 microseconds. Almost all stratum 2 and transit level and most stratum 3 and local clocks will reject a timing signal that has such a phase jump. Therefore, in most cases, the network clock will reject the timing signal when it experiences a pointer adjustment.

As discussed previously, DS1/E1 pointer adjustments can occur several times per day. Thus, if this signal is used for timing, the network clock will reject its timing reference and reference switch several times per day. This would add several microseconds of additional wander to the clock. Since ANSI and ITU require daily wander of less than 1 and 10 microseconds per day, respectively [8, 9], the network is in jeopardy of not meeting the standards.

All timing transfer with SDH/SONET is done by deriving timing from the optical carrier (Figure 5). The optical carrier is synchronous and free from pointer adjustments. A DS1 or E1 signal derived from this will be synchronized to the upstream SDH/SONET network element. The disadvantage of such an arrangement is that there can be additional clocking elements in the synchronization path.

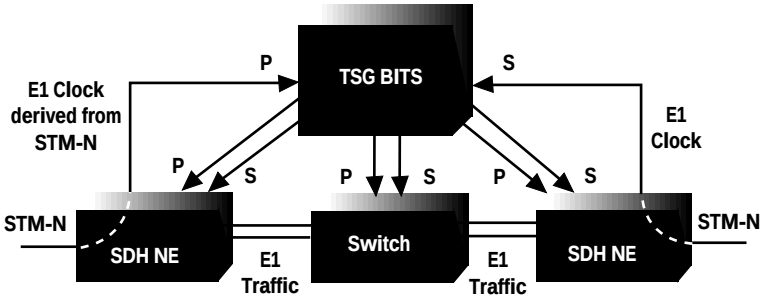


Figure 5. Timing distribution using SDH lines.

Private Network Customer DS1/E1 Service

As carriers introduce SDH/SONET into their networks, many private network services will be provisioned as payload on SDH or SONET systems. In these situations, all services for a private network location may be subjected to SDH/SONET pointer adjustments and the associated jitter and wander (Figure 6). Typically, the carrier's SDH or SONET equipment will not be on the customer's premises and the private network operator will not have access to the SDH/SONET timing signal derived from the optical carrier. The private network must rely on the SDH/SONET traffic signal for timing. This can cause problems, since the SDH/SONET payload is not suitable for timing transfer. This situation is currently under study in standards bodies and affected private network operators are handled on a case-by-case basis by the service provider.

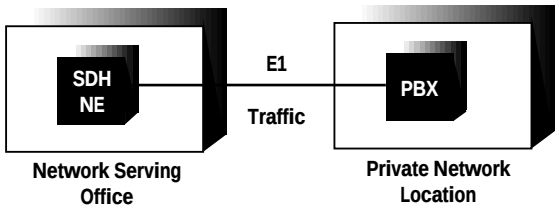


Figure 6. Private network service provided by SDH.

Network Requirements to Support SDH/SONET with DS1 or E1 Traffic

The wander introduced by SDH/SONET onto payload DS1/E1 causes the most stringent requirements to a network supporting SDH/SONET with DS1/E1. Two key performance requirements need to be met: low network wander in the 100- to 10,000-second range under ideal operation, and tight bounds on stress operation performance. The low network wander can be achieved by the use of stratum 3E or local level clocks. Tightening the bounds of stress operation performance is much more difficult.

Network performance under stress conditions is a function of facility performance, network clock performance, and synchronization architecture [1]. To limit stress operation performance, clock chains should be kept short, excellent facilities should be used, and the BITS/SSU clock should have excellent rearrangement MTIE specifications. The actual requirements will differ with each individual network.

As a guideline for stressed operation performance, consider a network with no more than three to four BITS/SSU clocks in a synchronization chain from the primary reference source (PRS) clock. Assume that the network uses excellent facilities with an average of two SES per day performance for its synchronization reference facilities. It would require that the BITS/SSU clocks have a 100-nanosecond rearrangement MTIE in order for it to support the DS1 wander budget for SONET transport. If the facility performance could not be guaranteed or the synchronization chains were longer, a better BITS/SSU clock would be needed.

VI. Synchronization Planning and SDH

The focus of synchronization planning is the determination of timing distribution and the selection of clocks and facilities used to time the network [2]. The distribution of timing and the selection of clocks are different between SDH and SONET networks. Therefore, this section will consider the synchronization planning needs of SDH networks. SONET networks will be the topic of the next section.

Reference Distribution

ITU provides a synchronization network reference connection (Figure 7) as a guideline for synchronization distribution [15]. In the chain, there should be no more than 10 transit or local nodes. These nodes refer to 10 offices that utilize a transit or local level clock as the SSU. Between offices are chains of SDH network element (NE) clocks. No one chain of SDH NE clocks should exceed 20 in number. The total number of SDH NE clocks in the entire reference connection should be less than 60. Each clock in the chain receives timing from the optical carrier as shown in Figure 5 on page 17.

This reference connection was determined based on simulations of operation under ideal conditions. It should meet the needs for maintaining 5-UI jitter levels for DS3, DS1, and E1 transport. Practical measurements have not been done to verify the simulations. It should be noted that the wander introduced on DS1 and E1 transport was not considered in this reference connection. The need to reduce wander levels by limiting stress operation performance may require a change to the reference connection as discussed in the previous section. Also, reliability concerns may require the length of the chain to be shortened.

SSU Clock Requirements

To meet the jitter requirements of DS3, DS1, and E1 transport through SDH, the SSU clock used to time the office in an SDH network should be at the transit or local level. The clock should have low intrinsic noise and should have a filter bandwidth of no more than 0.1 Hz to filter network noise. The clock is also required to have a rearrangement MTIE of 1,000 ns with a phase slope of less than 5×10^{-8} for most of its rearrangement period. This phase slope is considerably less than the phase slope requirements of SONET-based network clocks [8].

To limit E1 and DS1 wander, an SSU clock with considerably better rearrangement MTIE and increased filtering should be used. ITU has not yet developed guidelines for meeting DS1/E1 wander needs.

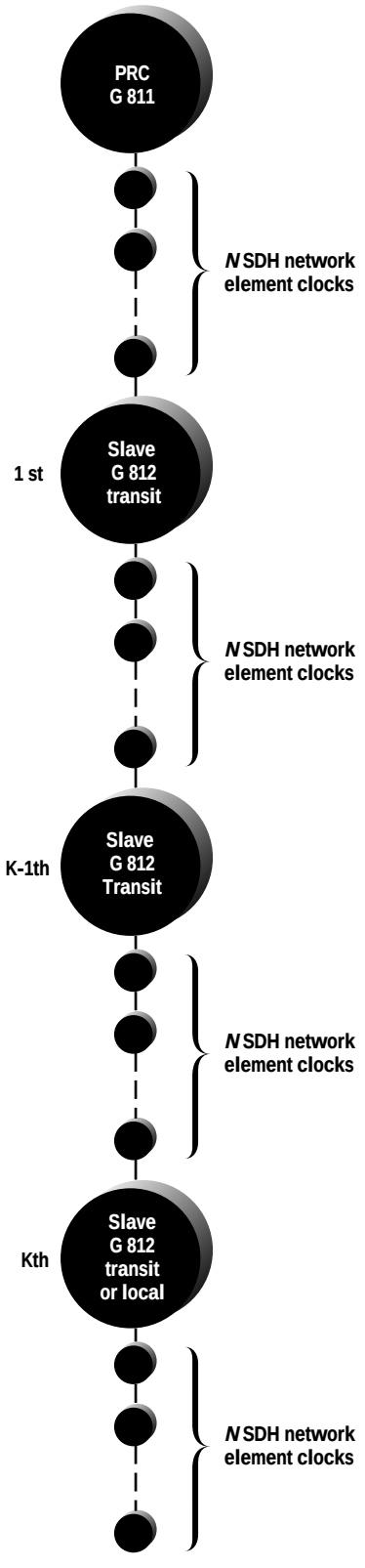


Figure 7. SDH synchronization network reference chain.

For worst-case scenario calculation purpose:

K = 10

N = 20 with restriction that total number of SDH network element clocks is limited to 60

SDH Network Element Clocking Requirements

The SDH network element (NE) clock is a poorer performing clock than the ITU local level clock. It has a holdover requirement of 5×10^{-8} for initial frequency offset and 5×10^{-7} per day for frequency drift. Its clock rearrangement requirements are an MTIE of less than 1.0 microseconds with a phase slope of less than 5×10^{-8} for most of its rearrangement period.

A major difference between the SDH NE clock and the SSU clock is the bandwidth of its design. The SDH NE clock has a bandwidth of 1 to 10 Hz. It is limited to this range for two reasons. First, the bandwidth must be at least 10 times the bandwidth of the SSU clock so that wander accumulation under ideal operating conditions is minimized. Second, the NE clock must support fast synchronization rearrangements.

When the SDH NEs are configured in a ring and a facility carrying synchronization is interrupted (Figure 8a), the synchronization distribution in the ring is reconfigured. The reconfigured distribution is shown in Figure 8b. The entire ring of 20 SDH NEs must reconfigure its synchronization distribution in about 15 seconds. This requires that each NE must reconfigure its synchronization and have a stable output within about one second. The one-second stability requirement limits how slowly the SDH NE can react, and hence, limits its filtering bandwidth.

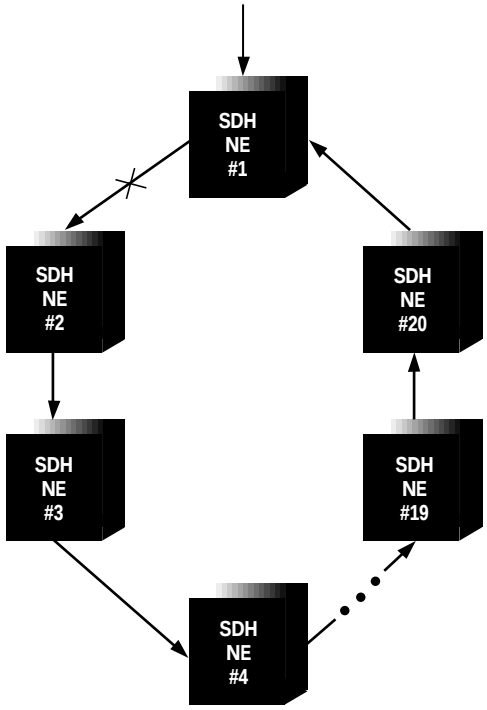


Figure 8a. SDH ring with normal timing flow counterclockwise.

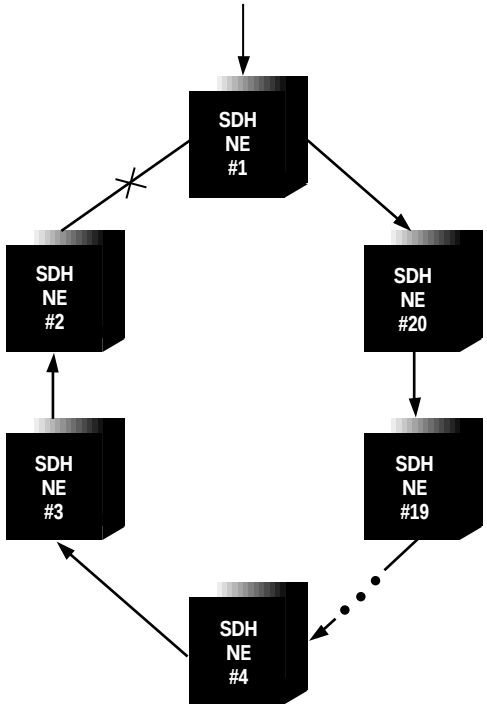


Figure 8b. SDH Ring with facility failure — timing flow clockwise.

VII. Synchronization Planning and SONET

In this section, we consider the synchronization planning needs of SONET networks. Synchronization planning involves the determination of timing reference distribution and the selection of clocks and facilities used in the synchronization network.

Reference Distribution

Synchronization distribution in SONET-based networks is different from distribution in SDH networks. In SONET networks, there are no SONET network elements (NEs) in the synchronization chain [6, 8]. The typical synchronization plan is given in Figure 9. The length of the synchronization chain is not specified by ANSI. However, most administrations will keep the synchronization chains short, with chain lengths of 1 to 6 being typical.

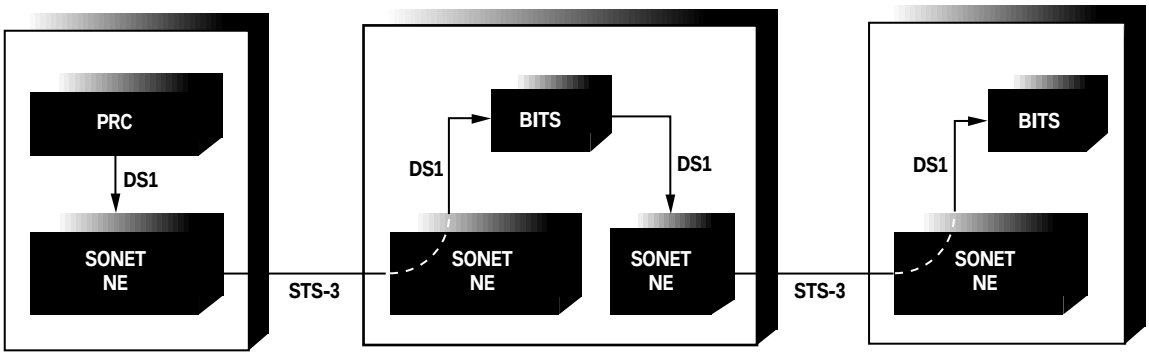
This synchronization network configuration, in conjunction with BITS and SONET NE clocks described in the following sections, should support error-free transmission of DS3, DS1, and E1 payloads.

BITS Clocks Requirements

The BITS clock needs to meet several requirements if it is to support SONET transport. First, the band-limited short-term noise should not exceed 17 nanoseconds [8]. Second, the BITS clock must filter noise below 100 seconds, as is implied by the ANSI output noise requirements. Third, to support DS1/E1 transport, the BITS clock requires low daily wander, implying that the BITS clock has excellent phase buildout and low MTIE during rearrangement.

To meet these requirements, it is recommended that the BITS clock be at the stratum 2 or 3E level and have exceptional rearrangement MTIE. The stratum 3E clock is a new clock, introduced by Bellcore [11] to meet the needs of SONET networks. A stratum 3E clock is between a stratum 2 and 3 in performance. It has the required noise filtering capabilities, a rearrangement MTIE of 100 ns, and the holdover capability of an ITU local clock. This clock is currently not accepted as a standard by ANSI. It does, however, provide a useful guideline for the minimum level of performance needed from a BITS clock.

Figure 9. Typical SONET network synchronization plan.



SONET Network Element Clocking Requirements

The clock in a SONET network element (NE) differs from the SDH NE clock primarily in its noise filtering. The SONET NE clock has a filtering bandwidth of 0.1 Hz, as compared to the 1 - 10 Hz bandwidth of the SDH NE clock. This is needed to filter the quicker phase transients of the BITS clocks (as compared to those of the SSU clock) and to filter network noise.

The SONET NE does not have the speed restriction of SDH. The synchronization rearrangement for a ring of 16 SONET NEs can occur over a 5-minute period. Similar to the SDH NE clock, the SONET NE has a holdover requirement of 5×10^{-8} for initial frequency offset and 5×10^{-7} per day for frequency drift. The SONET NE also has a clock rearrangement requirement of less than 1.0 microseconds MTIE with a phase slope of less than 9×10^{-7} for the first 0.5 seconds and 3×10^{-7} thereafter. Note that this phase slope is more lenient than that for SDH NE clocks.

VIII. Conclusions

The introduction of SDH and SONET presents greatly increased demands on network synchronization. The synchronization performance of most telecommunications networks requires improvement to support SDH and SONET. Short-term wander performance is crucial, requiring the use of excellent clocks. Stress operation performance also needs to be greatly limited. This requires the shortening of synchronization chains, necessitating the use of multiple primary reference clocks in many networks and the use of clocks with excellent rearrangement MTIE. All these actions are necessary to maintain acceptable transmission error rates for DS1, E1, and DS3 signals that pass through SDH and SONET.

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